FORM PTO-1449 (REV.7-80)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO. 500454.02	APPLICATION NO. Not yet assigned
		APPLICANT(S) Ronnie M. Harrison	
INFORMATION DISCLOSURE STATEMENT *(Use several sheets if necessary)*		FILING DATE Concurrently herewith	GROUP ART UNIT Not yet assigned

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
DXN	AA	4,984,255	01/08/91	Davis et al.	375	354	—
DXN	AB	5,341,405	08/23/94	Mallard, Jr.	375	376	—
DXN	AC	5,577,079	11/19/96	Zenno et al.	375	373	—
DXN	AD	6,087,857	07/11/00	Wang	327	5	—
DXN	AE	6,253,360 B1	06/26/01	Yoshiba	716	6	—
DXN	AF	6,285,726 B1	09/04/01	Gaudet	375	376	—
	AG						
	AH						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
	AK							
	AL							

OTHER PRIOR ART *(Including Author, Title, Date, Pertinent Pages, Etc.)*

DXN	AP	Descriptive literature entitled, "400MHz SLDRAM, 4M X 16 SLDRAM Pipelined, Eight Bank, 2.5 V Operation," SLDRAM Consortium Advance Sheet, published throughout the United States, pp. 1-22.
DXN	AQ	"Draft Standard for a High-Speed Memory Interface (SyncLink)", Microprocessor and Microcomputer Standards Subcommittee of the IEEE Computer Society, Copyright 1996 by the Institute of Electrical and Electronics Engineers, Inc., New York, NY, pp. 1-56.
DXN	AR	Maneatis, J., "Low-Jitter Process-Independent DLL and PLL Based on Self-Biased Techniques", IEEE Journal of Solid-State Circuits, Vol. 31, No. 11, November 1996, pp. 1723-1732.
DXN		Sidiropoulos, S. et al., "A Semidigital Dual Delay-Locked Loop", IEEE Journal of Solid-State Circuits, Vol. 32, No. 11, November 1997, pp. 1683-1692.

EXAMINER	DATE CONSIDERED
Dung X. Nguyen	10/01/2003

* EXAMINER: Initial if reference considered, whether or not criteria is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applican(s).